

What is claimed is:

- 1 1. An integrated circuit structure, comprising:
2 a capacitive electrode;
3 a dielectric underlying the capacitive electrode; and
4 an active region underlying the dielectric,
5 wherein the capacitive electrode and each conductive region between the
6 capacitive electrode and the active region are formed of a conductive material having a
7 hardness greater than a hardness of aluminum.
- 1 2. The integrated circuit structure of claim 1, wherein the capacitive electrode and
2 each conductive region between the capacitive electrode and the active region are formed
3 of a conductive material having a hardness at least as great as a hardness of the
4 dielectric.
- 1 3. The integrated circuit structure of claim 1, further comprising:
2 a passivation layer over the capacitive electrode,
3 wherein the capacitive electrode and each conductive region between the
4 capacitive electrode and the active region are formed of a conductive material having a
5 hardness at least as great as a hardness of the passivation layer.
- 1 4. The integrated circuit structure of claim 1, wherein the capacitive electrode and
2 each conductive region between the capacitive electrode and the active region are formed
3 of tungsten.
- 1 5. The integrated circuit structure of claim 4, further comprising:
2 a tungsten via beneath the capacitive electrode.
- 1 6. The integrated circuit structure of claim 5, further comprising:

2 a tungsten interconnect beneath the via.

1 7. The integrated circuit structure of claim 6, further comprising:
2 a tungsten contact between the interconnect and the active region.

1 8. The integrated circuit structure of claim 7, wherein the active region is a gate
2 electrode.

1 9. An integrated circuit structure, comprising:
2 an active region;
3 a dielectric overlying the active region and having a contact opening therethrough;
4 a tungsten contact within the contact opening;
5 a tungsten metal region overlying the contact and a portion of the dielectric;
6 an interlevel dielectric overlying the tungsten metal region and the dielectric and
7 having an opening therethrough;
8 a tungsten via within the opening through the interlevel dielectric; and
9 a tungsten capacitive electrode overlying the tungsten via and a portion of the
10 interlevel dielectric, wherein the capacitive electrode is electrically connected to the
11 active region by the contact, the metal region, and the via.

1 10. The integrated circuit structure of claim 9, further comprising:
2 an oxide over the capacitive electrode and the interlevel dielectric adjacent the
3 capacitive electrode;
4 a passivation layer including a silicon nitride layer and a silicon carbide layer over
5 the oxide; and
6 tungsten ESD protection within the passivation layer.

1 11. An integrated circuit, comprising:
2 an array of capacitive electrodes in a central portion of the integrated circuit; and
3 ESD protection devices and contact pads around a periphery of the integrated
4 circuit,

5 wherein the capacitive electrodes and every metallization region beneath the array
6 of capacitive electrodes within the central portion of the integrated circuit is formed of
7 a material having a hardness greater than aluminum while at least one metallization
8 region beneath an ESD protection device or contact pad is formed of aluminum.

1 12. The integrated circuit of claim 11, wherein every metallization region within the
2 central portion of the integrated circuit is formed of tungsten.

1 13. The integrated circuit of claim 12, further comprising:
2 tungsten ESD protection above and between capacitive electrodes within the array
3 of capacitive electrodes and within the central portion of the integrated circuit, wherein
4 each capacitive electrode within the array is formed of tungsten;
5 tungsten vias beneath each capacitive electrode;
6 tungsten interconnects beneath each tungsten via;
7 tungsten contacts beneath each tungsten interconnect; and
8 active regions beneath each tungsten contact.

1 14. A method of forming a scratch resistant integrated circuit structure, comprising:
2 forming an active region;
3 forming a dielectric overlying the active region; and
4 forming a capacitive electrode overlying the dielectric, wherein the capacitive
5 electrode and each conductive region between the capacitive electrode and the active
6 region are formed of a conductive material having a hardness greater than a hardness of
7 aluminum.

1 15. The method of claim 14, wherein the capacitive electrode and each conductive
2 region between the capacitive electrode and the active region are formed of a conductive
3 material having a hardness at least as great as a hardness of the dielectric.

1 16. The method of claim 14, further comprising:
2 forming a passivation layer over the capacitive electrode,
3 wherein the capacitive electrode and each conductive region between the
4 capacitive electrode and the active region are formed of a conductive material having a
5 hardness at least as great as a hardness of the passivation layer.

1 17. The method of claim 14, wherein the capacitive electrode and each conductive
2 region between the capacitive electrode and the active region are formed of tungsten.

1 18. The method of claim 17, further comprising:
2 forming a tungsten via beneath the capacitive electrode.

1 19. The method of claim 18, further comprising:
2 forming a tungsten interconnect beneath the via.

1 20. The method of claim 19, further comprising:
2 forming a tungsten contact between the interconnect and the active region.

1 21. The method of claim 20, wherein the active region is a gate electrode.

1 22. A method of forming an integrated circuit structure, comprising:
2 forming an active region;
3 forming a dielectric overlying the active region and having a contact opening
4 therethrough;
5 forming a tungsten contact within the contact opening;
6 forming a tungsten metal region overlying the contact and a portion of the
7 dielectric;
8 forming an interlevel dielectric overlying the tungsten metal region and the
9 dielectric and having an opening therethrough;
10 forming a tungsten via within the opening through the interlevel dielectric; and
11 forming a tungsten capacitive electrode overlying the tungsten via and a portion
12 of the interlevel dielectric, wherein the capacitive electrode is electrically connected to
13 the active region by the contact, the metal region, and the via.

1 23. The method of claim 22, further comprising:
2 forming an oxide over the capacitive electrode and the interlevel dielectric
3 adjacent the capacitive electrode;
4 forming a passivation layer including a silicon nitride layer and a silicon carbide
5 layer over the oxide; and
6 forming tungsten ESD protection within the passivation layer.

1 24. A method of forming a scratch resistant integrated circuit structure, comprising:
2 forming a plurality of active regions;
3 forming a dielectric over the plurality active regions; and
4 forming an array of capacitive electrodes overlying the dielectric of a conductive
5 material having a hardness at least as great as a hardness of the dielectric.

1 25. The method of claim 24, wherein the step of forming an array of capacitive
2 electrodes overlying the dielectric of a conductive material having a hardness at least as
3 great as a hardness of the dielectric further comprises:
4 forming the array of capacitive electrodes of a conductive material having a
5 hardness at least as great as a hardness of a passivation layer overlying the array of
6 conductive electrodes.

1 26. The method of claim 24, wherein the step of forming an array of capacitive
2 electrodes overlying the dielectric of a conductive material having a hardness at least as
3 great as a hardness of the dielectric further comprises:
4 forming the array of capacitive electrodes of tungsten.

1 27. The method of claim 24, further comprising:
2 forming each metallization region between the array of capacitive electrodes and
3 the plurality of active regions of a conductive material having a hardness at least as great
4 as the hardness of the dielectric.